Remarks

Reconsideration of this Application is respectfully requested.

Claims 8-42 are pending in the application, with claims 8, 20 and 28 being the independent claims.

Based on the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Nonstatutory Double Patenting Rejections

The Examiner has rejected claims 8 and 20 on the ground of nonstatutory obviousness-type double patenting. In particular, the Examiner has rejected claim 8 as being unpatentable over claim 46 of U.S. Patent No. 6,092,181, claim 14 of U.S. Patent No. 6,647,485, claim 65 of U.S. Patent No. 6,038,654, and claim 8 of co-pending U.S. Patent Application No. 10/700,485. The Examiner has rejected claim 20 as being unpatentable over claim 8 of U.S. Patent No. 6,256,720.

On December 28, 2004, Applicants filed in the present case a Terminal Disclaimer to Obviate a Double Patenting Rejection Over U.S. Patent Nos. 5,539,911, 5,689,720, 6,092,181, 6,038,654, 6,256,720 and 6,647,485 and a Terminal Disclaimer to Obviate a Provisional Double Patent Rejection Over U.S. Patent Application Nos. 10/282,045, 10/282,207, 10/283,177, 10/283,106, 10/697,257, 10/700,485 and 10/700,520. Applicants respectfully submit that the filing of these Terminal Disclaimers overcomes the Examiner's obviousness-type double patenting rejections. Accordingly,

Applicants request that the rejection of claims 8 and 20 on the ground of nonstatutory obviousness-type double patenting be reconsidered and withdrawn.

Rejections under 35 U.S.C. § 103

Claims 8-14, 19-24, 28-34, 39 and 40-42

The Examiner has rejected claims 8-14, 19-24, 28-34, 39 and 40-42 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,488,729 to Vegesna *et al.* ("Vegesna") in view of U.S. Patent No. 4,200,927 to Hughes *et al.* ("Hughes")[1]. For the reasons set forth below, Applicants respectfully traverse.

Independent claim 8 is directed to a superscalar microprocessor for processing instructions having a program order. The microprocessor of claim 8 includes:

> a fetch circuit configured to fetch instructions, including a conditional branch instruction, from an instruction store;
>
> a branch detection circuit configured to detect the conditional branch instruction from among the fetched instructions;
>
> a branch bias circuit configured to receive a branch bias signal indicating whether a conditional branch controlled by the conditional branch instruction is predicted to be taken or not taken;
>
> a stream identifier circuit configured to associate a stream identifier with one or more of the fetched instructions, thereby identifying a first stream predicted by the branch bias signal;
>
> a buffer circuit configured to receive and buffer the fetched instructions;

[1] At page 4 of the Office Action, the Examiner indicated that claim 15 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Vegesna in view of Hughes. However, the Examiner provided no basis for this rejection of claim 15. Rather, the Examiner later provided an argument that claim 15 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Vegesna in view of Hughes and further in view of U.S. Patent No. 5,394,529 to Brown III *et al.* ("Brown"). *See* Office Action at pages 6-7. Accordingly, Applicants will assume that the Examiner intended to reject claim 15 over the three-way combination of Vegesna, Hughes and Brown rather than over the two-way combination of Vegesna and Hughes.

> a decode circuit coupled to the buffer circuit and configured to make a group of buffered instructions concurrently available for execution as decoded instructions, wherein the available decoded instructions include a decoded instruction corresponding to the conditional branch instruction and a decoded instruction from the first stream; and
>
> an execution circuit including a plurality of functional units configured to execute the available decoded instructions out of the program order, wherein execution of the conditional branch instruction determines whether the conditional branch is taken,
>
> wherein the fetch circuit is further configured to cancel instructions from the first stream based on the stream identifier in the event that the branch bias signal incorrectly predicts whether the conditional branch is taken.

The combination of Vegesna and Hughes does not teach or suggest each and every one of the foregoing features of claim 8.

For example, neither Vegesna or Hughes teaches or suggests "a stream identifier circuit configured to associate a stream identifier with one or more of the fetched instructions, thereby identifying a first stream predicted by [a] branch bias signal" and a fetch circuit that is configured to "cancel instructions from the first stream based on the stream identifier in the event that the branch bias signal incorrectly predicts whether [a] conditional branch is taken" as recited by claim 8. The Examiner has conceded that Vegesna does not teach or suggest these features. As will be discussed in more detail below, although Hughes does describe the buffering of multiple instruction streams for the purposes of branch processing in a microprocessor, it also does not teach or suggest these particular features.

Hughes teaches an Instruction Preprocessor Function (IPPF) 20 that includes "three separate instruction buffers, each capable of storing a plurality of instructions from three separate instruction streams to be utilized, one at a time, in [an] instruction predecode mechanism 28." *See* Hughes, col. 4, lines 1-5. As described in Hughes:

> In accordance with the present invention, the IPPF mechanism includes three separate instruction-fetching mechanisms referred to as instruction streams A, B, and C. Each instruction stream includes an instruction address register (Instruction counter) and a set of four, double-word buffers for storing prefetched instructions from storage. The prefetching of instructions into the instruction buffers and selection of one of the three instruction buffers for gating of individual instructions to an instruction decoding register is controlled by logic which keeps track of the status of each instruction stream, allocates instructions streams to target instruction streams, deallocates or resets instruction stream based on the results of conditional branch instructions, and manages a set of instruction stream pointers that control stream-related activities throughout the IPPF.

See Hughes, col. 2, lines 39-54. Thus, in Hughes, instruction streams are distinguished for the purposes of branch processing by their assignment to one of three instruction buffers (I-Buffers A, B and C). Consequently, the identification of which stream an instruction belongs to is based on the *physical location* of an instruction in one of the three buffers.

This is very different approach from that recited in claim 8, in which a stream identifier circuit associates a "stream identifier" with one or more fetched instructions, and the stream identifier (as opposed to the physical location of the instruction) is thereafter used to identify whether or not an instruction belongs to a particular stream of instructions. In particular, the fetch circuit of claim 8 uses the stream identifier to "cancel instructions from the first stream based on the stream identifier in the event that the branch bias signal incorrectly predicts whether [a] conditional branch is taken". By using a "stream identifier" in this manner, an embodiment of the present invention can store instructions from one stream of instructions with other instructions that are not part of the same stream in the same buffer. Hughes does not use "stream identifiers" as recited by claim 8 and thus cannot provide this functionality. Rather, Hughes must isolate each instruction stream into a separate dedicated buffer.

Since the combination of Vegesna and Hughes fails to teach or suggest each and every feature of independent claim 8, the combination cannot render claim 8 obvious. Dependent claims 9-14, 19 and 40 are likewise not rendered obvious by the combination of Vegesna and Hughes for the same reasons as independent claim 8 from which they depend and further in view of their own respective features. Accordingly, Applicants respectfully request that the rejection of claims 8-14, 19 and 40 under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

Independent claim 20 is directed to a method in a superscalar microprocessor for processing instructions having a program order that includes the steps of "associating a stream identifier with one or more . . . fetched instructions, thereby identifying a first stream predicted by [a] branch bias signal" and "in the event that the branch bias signal incorrectly predicted whether [a] conditional branch is taken, canceling instructions from the first stream based on the stream identifier". For the reasons set forth above in regard to independent claim 1, neither of these features are taught or suggested by Vegesna or Hughes. Consequently, the combination of Vegesna and Hughes cannot render cannot render claim 20 obvious. Dependent claims 21-24 and 41 are likewise not rendered obvious by the combination of Vegesna and Hughes for the same reasons as independent claim 20 from which they depend and further in view of their own respective features. Accordingly, Applicants respectfully request that the rejection of claims 20-24 and 41 under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

Independent claim 28 is directed to a computer system that includes a microprocessor, the microprocessor including "a stream identifier circuit configured to associate a stream identifier with one or more of the fetched instructions, thereby

identifying a first stream predicted by the branch bias signal" and a fetch circuit that is configured to "cancel instructions from the first stream based on the stream identifier in the event that the branch bias signal incorrectly predicts whether [a] conditional branch is taken". For the reasons set forth above in regard to independent claim 1, neither of these features are taught or suggested by Vegesna or Hughes. Consequently, the combination of Vegesna and Hughes cannot render cannot render claim 28 obvious. Dependent claims 29-34, 39 and 42 are likewise not rendered obvious by the combination of Vegesna and Hughes for the same reasons as independent claim 28 from which they depend and further in view of their own respective features. Accordingly, Applicants respectfully request that the rejection of claims 28-34, 39 and 42 under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

Claims 15, 17, 25, 26 and 35-37

The Examiner has rejected claims 15, 17, 25, 26 and 35-37 under 35 U.S.C. § 103(a) as being unpatentable over Vegesna in view of Hughes and further in view of U.S. Patent No. 5,394,529 to Brown III *et al.* ("Brown"). As discussed above, neither Vegesna nor Hughes teaches or suggests the features of independent claims 8, 20 and 28 relating to the association of a stream identifier with one or more fetched instructions, thereby identifying a first stream predicted by a branch bias signal, or the cancellation of instructions from the first stream based on the stream identifier in the event that the branch bias signal incorrectly predicted whether a conditional branch is taken. Brown does not supply the missing teaching or suggestion. Consequently, the combination of Vegesna, Hughes and Brown cannot render independent claims 8, 20 and 28 obvious.

Dependent claims 15, 17, 25, 26 and 35-37 are likewise not rendered obvious by this combination for the same reasons as the independent claims from which they depend and further in view of their own respective features. Accordingly, Applicants respectfully request that the rejection of claims 15, 17, 25, 26 and 35-37 under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

Other Matters

The Examiner has objected to claims 16, 18, 27 and 38 as being dependent upon a rejected base claim. By virtue of the foregoing Remarks, the rejection of the base claims upon which these claims depend has been traversed. Accordingly, Applicants respectfully request that the objection to claims 16, 18, 27 and 38 be reconsidered and withdrawn.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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